1. Refer to Exercise 1 Task 3. Consider a cell switch with N input and output ports. In each time-slot at each input port, the probability that that a cell arrives is p. The incoming traffic is uniformly distributed, i.e., the probability that an incoming cell is destined to any output port is $1/N$.

   (a) In the case that there is no buffering, only one of the cells arriving in a specific port can pass while others are lost. What is the average number of lost cells? Give an example for 8x8 ($N = 8$) switch at full load ($p = 1$).

   (b) Loss probability can be reduced by using buffering. If buffers are placed at output ports, they must operate at higher speed than the line-speed. How many cells an output buffer should accept during one time-slot to keep the average number of lost cells due to output port blocking below 10^{-5} when $N = 8$ and $p = 0.85$?

2. A time switch is implemented using the principle given below:

   - Incoming time-slots are written cyclically into a switch memory (SM)

   - Output logic reads cyclically control memory (CM), which contains a pointer for each output time-slot

   Inputs and outputs as well as read/write logic of the memories are expected to be in synchronism.

   What are the required speeds of SM and CM if the switching is dimensioned to support 120 input and output E1-links. What are required memory sizes of SM and CM? What about the sizes of input and output buffers? Suppose that SM and CM are shared by all E1s and that there is a memory slot for each time-slot.

3. Time switch principle can also be used to implement a cell switch. In this case whole cells are switched at time instead of (1-octet) time-slots, i.e., the length of a time-slot is one cell. Furthermore, no cells should be lost in the switch core and the order of the cells should no be alterered. CM is replaced by a control unit that schedules the operations. Describe the principles of the scheduling and what changes are required to SM if any. You may assume that each input port has a non-blocking input buffer.

4. Consider a 3-stage circuit switched symmetric Clos switching matrix with 512 input lines. Each input has an average holding time of 260 s and input rate of 1/320 1/s.

   (a) The input is divided into 32 blocks of type 16xk, where k is number of 2nd stage blocks. Use Lee's approximation to find out such k that the blocking probability is < 0.001. What is the total number of switching points?

   (b) What the value of k and the number of the blocks if the switch must be strictly non-blocking?