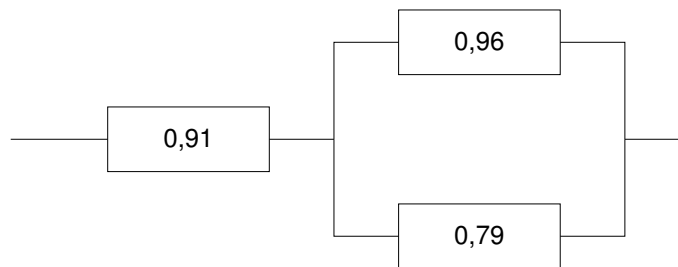


1. Consider a switch with 8 STM-16 (that is 16 times STM-1 rate) ports using central memory buffering. Only the payload of the SDH frames are stored and retrieved from the buffer.
 - (a) What is the required memory bandwidth?
 - (b) If 133 MHz SDRAM modules are used, what is the width of the memory bus? If each module is 64-bit wide, how many modules are required in parallel?
 - (c) If 32-bit wide 400 MHz dual data-rate (DDR) (that is at each clock cycle two words can be read, so the data rate is 800 MHz) SRAM devices are used, what is the width of memory bus and how many devices are required in parallel.
 - (d) Compare the scalability of SDRAM and DDR-SRAM solutions if the capacity for SDRAM module is 256 MB and DDR-SRAM device 1 Mbit.
2. What is the reliability of the system below? What is the optimal place to add a spare module (reliability = 0.93) and what is the new reliability that is achieved?



3. Consider a system with two redundant units in parallel. Both the active and standby units are energised. For both units the failure rate is $\lambda = 1/100$ days and the repair rate is $\mu = 1/6$ hours. If the active unit fails, the standby unit takes its tasks and the failed unit undergoes repairs. Make a Markov model for the system, form the equilibrium equations (as functions of λ and μ) and solve the state probabilities for each of the states. Note that if the both units have failed they are repaired consecutively.
4. Consider a SDH transmission chain in the figure below. Each SDH element has own clock (CK1-CK5) with different deviations (shown in the figure) from the nominal frequency (ppm = parts per million = 10^{-6}). The differences in local clock signals can be made up with AU pointer justifications. Let's assume that a VC-4 container is transmitted in STM-4 frame. In that case AU-4 pointer justification is used and it recovers a phase offset of 24 bits at time. What is the frequency of pointer justifications at points A, B, C, and D?

